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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/720,502	04/27/2001	Martyn Gilbert	UDL-5648	3390

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EXAMINER	
VU, THONG H	

ART UNIT	PAPER NUMBER
2142	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/720,502	GILBERT, MARTYN	
	Examiner	Art Unit	
	Thong H. Vu	2142	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-25 and 33-36 are canceled. Claims 25-32 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 26-32 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 26-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiiragizawa [5,561,390].

3. Claim 26 Hiiragizawa discloses A device having at least first and second communications sections suitable for connection to similar devices along different bi-directional communications links [Hiiragizawa, a phase lock loop circuit, Fig 1],

said first communications section being arranged to respond to reception of a clock transition signal along a first communications link by transmitting a clock transition signal having the same polarity back along said first communications link [Hiiragizawa, first node with clock signal and first polarity, col 10 lines 7-31], and

said second communications section arranged to respond to reception of a clock transition signal along a second communications link by transmitting a clock transition

signal having the opposite polarity back along said second communications link [Hiiragizawa, second node with opposite polarity, col 10 lines 7-31].

4. Claim 27, Hiiragizawa discloses said first communications section holds a first clock logic level and an output, when the first communications section is not connected to another device, and wherein said second communications section holds a second clock logic level having an opposite polarity to the first clock state logic level as an input, when the second communications section is not connected to another device [Hiiragizawa, clock state level, col 3 lines 40-55].

5. Claim 28, Hiiragizawa discloses said second communications section holds a first clock logic level as an output, when the second communications section is not connected to another device, and wherein said first communications section holds a second clock logic level having an opposite polarity to the first clock state logic level as an output, when the first communications section is not connected to another device [Hiiragizawa, clock state level, col 3 lines 40-55].

6. Claim 29, Hiiragizawa discloses the linked communication sections form a loop, when the first communications section is linked to the second communications section of another device or vice-versa through a bi-directional communications link, and wherein the device uses an oscillating clock transition signal passing around the loop as

a clock signal for communication along the communications link as inherent features of phase lock loop.

7. Claim 30 Hiiragizawa discloses the first and second communication sections are first linked, the difference between their held input and output clock logic levels causes the oscillating clock transition signals to begin passing around the loop as inherent features of phase lock loop.

8. Claim 31 Hiiragizawa discloses An electronic communication network comprising at least first and second devices connected by at least one bi-directional communications link [Hiiragizawa, a phase lock loop circuit, Fig 1],

wherein a loop is formed by said first device receiving a clock transition signal along the communications link and sending a clock transition signal having the same polarity back along the communications link and said second device receiving a clock transition signal along the communications link and sending a clock transition signal having the opposite polarity back along the communications link [Hiiragizawa, first node with clock signal and first polarity, col 10 lines 7-31], and

wherein the first and second devices use the oscillating clock transition signals traveling around the loop to provide a clock signal to control data transfer along the communications link [Hiiragizawa, second node with opposite polarity, col 10 lines 7-31].

9. Claim 32, Hiiragizawa discloses the clock transition signals traveling around the loop are used as said clock signal as inherent features of phase lock loop.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner *Thong Vu*, whose telephone number is (571)-272-3904. The examiner can normally be reached on Monday-Thursday from 6:00AM- 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Andrew Caldwell*, can be reached at (571) 272-3868. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval IPAIRI system. Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Vu
Primary Examiner
Art Unit 2142